**Win Condition:**

The win condition module tracks the scores of each player and sets flags to stop the game and display which player won. The inputs for the win condition entity are: clk, reset, pulse, scoreA, and scoreB. The outputs are hold and winner.

entity win\_logic is

port (

clk : in std\_logic;

reset : in std\_logic;

pulse : in std\_logic;

scoreA, scoreB : in std\_logic\_vector(3 downto 0);

hold : out std\_logic;

winner: out std\_logic\_vector(1 downto 0)

);

end entity;

The win condition entity was implemented with a finate state machine that consisted of three states: idle, delay, and endgame. The idle state does nothing, waiting for a pulse to be detected by the entity. Once a pulse has been detected, scoreA and scoreB are compared to the constant SCORE\_TO\_WIN. If scoreA has reached the winning condition, the win signal is set to “01”, the encoding for player A winning the game. If player B has won the game, the win signal is set to “10”. The win signal is default set to “00” which indicates no player has achieved victory yet. This output is fed into the lcd entity which will display the name of player that has won. Once a win is detected, the entity enters the delay state. The delay state just waits for the pulse to drop to ‘0’ so that the rest of the game can finish computation. At this point the state is set to endgame. In the endgame state, the hold signal is raised to high. This signal is used to stop the counter, effectively stopping the game.